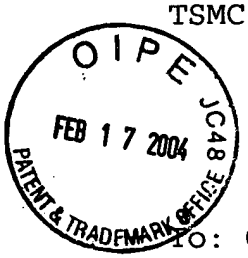
TSMC-03-299



February 9, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/714,985 11/17/03

William Hong et al.

COPPER CMP DEFECT REDUCTION BY EXTRA SLURRY POLISH

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February , 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B Acker 2/12/04

U.S. Patent 6,503,828 to Nagahara et al., "Process for Selective Polishing of Metal-Filled Trenches of Integrated Circuit Structures," describes a method to prevent dishing.

U.S. Patent 6,395,635 to Wang et al., "Reduction of Tungsten Damascene Residue," discusses a three step CMP process followed by a two step buffing procedure applied to a dielectric layer to reduce residue and scratch defects on a tungsten damascene structure.

U.S. Patent 6,153,526 to Shih et al., "Method to Remove Residue in Wolfram CMP," discloses a method for removing residue in a tungsten CMP process.

U.S. Patent 6,432,826 to Emami et al., "Planarized Cu Cleaning for Reduced Defects," discloses a planarizing method for copper with reduced defects.

Co-pending U.S. Patent TSMC-02-992, "An Advanced Process Control Approach for Cu Interconnect Wiring Sheet Resistance Control," Serial # 10/723,236, filed on 11/26/03, assigned to the same assignee, discusses a method of performing a chemical mechanical polishing step on copper wiring with a higher degree of process control to enable copper sheet resistance to be minimized.

Co-pending U.S. Patent TSMC-03-424, "Barrier-Slurry-Free Copper CMP Process," Serial # 10/627,795, filed on 7/25/03, assigned to a common assignee, discusses a method of reducing the number of defects on a substrate following a chemical mechanical polishing (CMP) step of a copper interconnect structure.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-03-299	10/714,985
Applicant: William Hong et al.	
Filing Date: 11/17/03	Group Art Unit

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6503828	1/7/03	Nagahara et al.	438	633	6/14/01
	6395635	5/28/02	Wang et al.	438	692	12/7/98
	6153526	11/28/00	Shih et al.	438	692	5/27/99
	6432826	8/13/02	Emami et al.	438	692	11/29/99

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- Co-pending U.S. Patent TSMC-02-992, Serial # 10/723,236, filed on 11/26/03, same assignee, "An Advanced Process Control Approach for Cu Interconnect Wiring Sheet Resistance Control"
- Co-pending U.S. Patent TSMC-03-424, Serial # 10/627,795, filed on 07/25/03, same assignee, "Barrier-Slurry-Free Copper CMP Process".

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.